EECS3342 System Specification and Refinement (Winter 2022)

Q&A - Week 7 Lectures

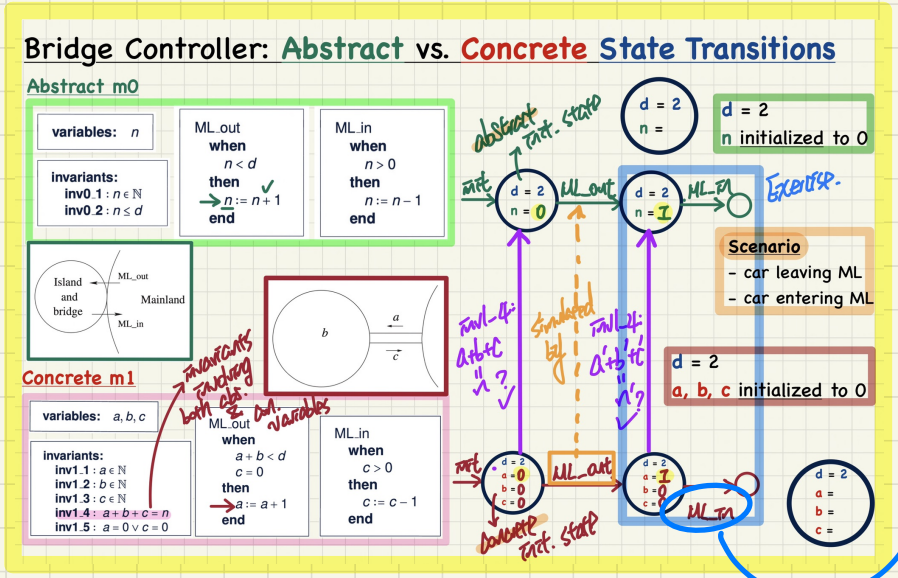
Thursday, March 10

Announcements

W9 (4).

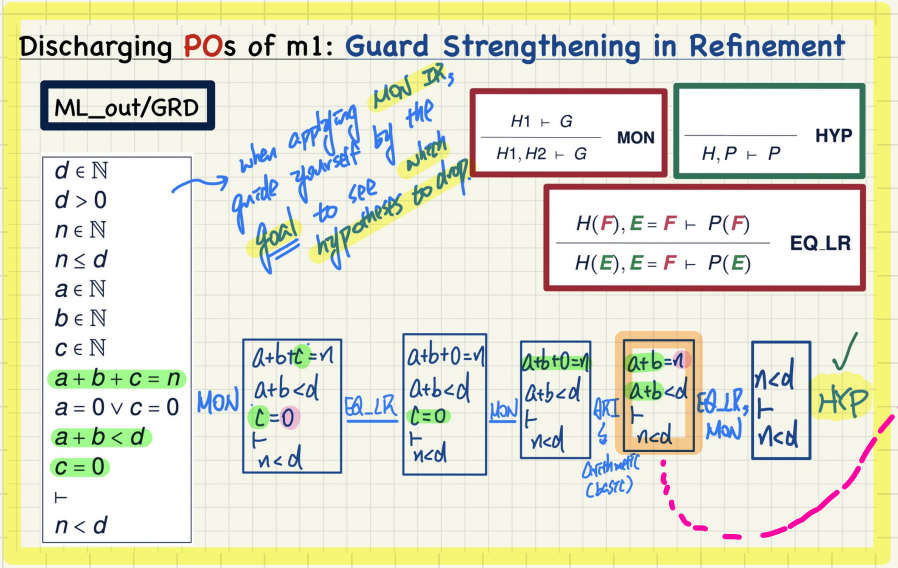
+ No Lecture W8 released
+ Written Test 3

Towards the end of this lecture, you stated that there had to be a concrete representation of ML_in.
I was wondering how this would work since c = 0 in this case.
For the abstract model, we can execute ML_in since n = 1 after the ML_out event, but in the case for m1, c = 0 since the bridge is one way.



1. disabled : c=0
2. try adding some transitions by IL_in & IL_out

For the following dischargement,
you used EQ_LR twice to achieve n < d ⊢ n < d.
I was wondering if it would also be valid to use EQ_RL the second time to achieve a + b < d ⊢ a + b < d?
Would this be bad practice?
How would that be marked in a test setting?



$$\frac{H, \neg P \vdash Q}{H \vdash P \vee Q}\ \text{OR\_R}$$

disjunctive goal

$H \Rightarrow P \vee Q$

$\equiv H \wedge \neg P \Rightarrow Q$

extra hypothesis

(¬ of one of the goal(s))

$d > 0$
$a \in \mathbb{N}$
$b \in \mathbb{N}$
$\vdash$
$\quad . \ a + b < d \wedge 0 = 0$
$\vee \cdot \ 0 > 0$
$\vee \ a > 0$
$\vee . \ b > 0 \wedge a = 0$

OR_R

$d > 0$
$a \in \mathbb{N}$.
$b \in \mathbb{N}$
$\neg(a > 0)$
$\vdash$
$a + b < d \wedge 0 = 0$
$\vee \ 0 > 0$
$\vee \ b > 0 \wedge a = 0$

$a = 0$